Appendix A. Identification of Amended Material

The paragraphs encompassing page 1, line 12 - page 2, line 16 are amended as follows:

The present invention provides an electronic structure, comprising:

an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

a redistribution structure having N dielectric layers denoted as dielectric layers 1, 2, ..., N, N metal planes denoted as metal planes 1, 2, ..., N, and a microvia structure through the N dielectric layers, wherein N is at least 2, wherein dielectric layer 1 is on the first surface of the substrate and on the metallic plane, wherein metal plane J is on dielectric layer J for J =1, 2, ..., N, wherein dielectric layer I is on dielectric layer I-1 and on metal [layer] plane I-1 for I = 2, ..., N, and wherein the microvia structure electrically couples metal plane N to the metallic plane. metallic plane.

The present invention provides a method for forming an electronic structure, comprising:

providing an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

forming a redistribution structure including forming N dielectric layers denoted as dielectric layers 1, 2, ..., N, forming N metal planes denoted as metal planes 1, 2, ..., N, and forming a microvia structure through the N dielectric layers such that the microvia structure electrically couples metal plane N to the metallic plane, wherein N is at least 2, and wherein forming the N dielectric layers and the N metal [layers] planes includes setting a dummy index J=0 and looping over J as follows:

adding 1 to J;

if J = 1 then forming dielectric layer 1 on the first surface of the substrate and on the metallic plane, else forming dielectric layer J on dielectric layer J-1 and on metal plane J-1;

forming metal plane J on dielectric layer J; and

if J < N then returning to adding 1 to J and continuing the looping, else ending the looping.

The paragraph beginning on page 13, line 4 is amended as follows:

FIG. 2 illustrates advantages of the multiple redistribution layers (e.g., the redistribution layers **60**, **70**, **80**, and **90**) on the top surface **48** and on the bottom surface **49** of the substrate **10**. The redistribution layers serve as buildup layers which provides a capability of adding extra wiring layers; e.g., the metal planes **140-141** and **150-151**. The extra wiring level, coupled with the microvias (e.g, the microvias **132-135** and **144-148**) in the multiple redistribution layers, provide extra wireout capability for making more efficient use of space and increasing overall wiring density. In addition, there is increased flexibility in how electrically conductive structure may be distributed inasmuch as a metal plane on each redistribution layer may be any metal distribution, included a signal plane, a power plane, or a ground plane. With the multiple redistribution layers, any metal [level] <u>or metallic plane</u> on a redistribution layer on the top surface **48** of the substrate **10** may be electrically coupled to any metal [level] <u>or metallic plane</u> on a redistribution layer on the bottom surface **49** of the substrate **10** or to any internal layer of the substrate **10**, in light of the electrically conductive paths facilitated by the microvias in the redistribution layers **60**, **70**, **80**, and **90** and the PTHs in the substrate **10**. FIG. 2 illustrates several

of such electrically conductive paths. For example, the metal plane **140** is electrically coupled to the metal plane **151** through the path of the conductive region **137**, the microvia **133**, the conductive pad **42**, the PTH **32**, the conductive pad **45**, the microvia **135**, and the microvia **148**. As another example, the electronic device **110** is coupled to the conductive pad **44** of the PTH **31** by a path that includes the conductive pad **128**, the solder member **121**, the microvia **145**, the conductive pad **131**, the microvia **132**, the conductive pad **41**, the PTH **31**, and the conductive pad **44**. The electronic device **110** may be coupled to wiring in the redistribution layer **70** through the solder member **122** and the microvia **146**, or to wiring in the redistribution layer **60** through the solder member **120** and the microvia **144** or through the solder member **121** and the microvias **145** and **132**. The number and types of conductive paths facilitated by the multiple redistribution layers of the present invention are virtually unlimited. FIG. 3 also includes the aforementioned features and advantages.

The paragraph beginning on page 15, line 11 is amended as follows:

As illustrated for the embodiments of FIGS. 2 and 3, the multiple redistribution structure on either the top surface **48** or the bottom surface **49** of the substrate **10** has N dielectric layers (denoted as dielectric layers 1, 2, ..., N) , N metal planes (denoted as metal planes 1, 2, ..., N), and a microvia structure, wherein $N \geq 2$. Dielectric layer 1 (i.e., redistribution layer **60** or **80**) is on the top surface **48** or the bottom surface **49** of the substrate **10** and thus also on a metallic plane; i.e., on the metal plane **51** or the metal plane **52**, respectively. Thus, the metals planes **51** and **52** are each called a "metallic plane" for purposes of the notation being discussed herein. Metal [level] plane 1 (i.e., metal plane **140** or **141**) is on dielectric layer 1, dielectric layer 2 (i.e., redistribution

layer 70 or 90) is on dielectric layer 1 and metal [layer] plane 1, metal [layer] plane 2 (i.e., metal plane 150 or 151) is on dielectric layer 2, ..., dielectric layer N is on dielectric layer N-1 and metal [layer] plane N-1, and metal [layer] plane N is on dielectric layer N. The microvia structure electrically couples the metal [layer] plane N to the metallic plane (i.e., the metal plane **51** or the metal plane **52**) by a collection of microvias coupled with intervening metal [levels] planes. The microvia structure includes a microvia or a portion of a microvia through each of the N dielectric layers. Many such combinations of microvias are possible. An example microvia combination is N microvias (i.e., a microvia in each dielectric layer) such that microvia J is electrically coupled to microvia J-1 by metal plane J-1 for J=2, 3, ..., N. To illustrate, FIG. 3 has N=3 and shows: microvia **345** electrically coupled to microvia **385** by metal plane **380** (specifically, conductive pad **386** in metal plane **380**), microvia **385** electrically coupled to microvia **334** by metal plane **340** (specifically, conductive pad **338** in metal plane **340**), and microvia **334** electrically coupled to metal plane **51** by conductive pad **33**, which electrically couples the metal plane **395** to the metal plane **51** in light of the fact that conductive pad **346** of metal plane **395** is integral with, and thus electrically connected with, the conductive plating of the microvia **346**. Another microvia combination includes a microvia that passes through two or more dielectric layers (e.g., the microvia **144** of FIG. 2). For example and although not shown explicitly in FIG. 3, a microvia could pass through redistribution layers **360**, **370**, and **390**, or through redistribution layers **370** and **390**, just as microvia **144** of FIG. 2 passes through redistribution layers **60** and **70**. Thus in FIG. 3, a microvia passing through redistribution layers **370** and **390** could be electrically coupled by metal plane **340** to a microvia (e.g., the microvia **332**, **333**, or **334**) in redistribution layer **360**.

Claims 1, 2, 6, 19, and 22 are amended as follows:

1. (AMENDED) An electronic structure, comprising:

an internally circuitized substrate having a metallic plane on a first surface of the substrate; and

a redistribution structure having N dielectric layers denoted as dielectric layers 1, 2, ..., N, N metal planes denoted as metal planes 1, 2, ..., N, and a microvia structure through the N dielectric layers, wherein N is at least 2, wherein dielectric layer 1 is on the first surface of the substrate and on the metallic plane, wherein metal plane J is on dielectric layer J for J =1, 2, ..., N, wherein dielectric layer I is on dielectric layer I-1 and on metal [layer] plane I-1 for I = 2, ..., N, and wherein the microvia structure electrically couples metal plane N to the metallic plane.

2. (AMENDED) The electronic structure of claim 1, wherein the microvia structure includes N microvias denoted as microvias 1, 2, ..., N, wherein the microvia K passes through dielectric layer K for K = 1, 2, ..., N, wherein metal plane N is electrically coupled to microvia N, wherein metal plane J-1 electrically couples microvia J to microvia J-1 for J = 2, 3, ..., N, and wherein microvia 1 is electrically coupled to the metallic plane.

6. (AMENDED) The electronic structure of claim 4, wherein the microvia structure further includes M-1 second microvias denoted as second microvias 1, 2, ..., M-1, and wherein the second microvia K passes through dielectric layer K for K = 1, 2, ..., M-1, wherein the metal plane M-1 electrically couples the first microvia to second microvia M-1, wherein if M > 2 then metal plane J-1 electrically couples second microvia J to second microvia J-1 for J = 2, 3, ..., M-1, and

wherein second microvia 1 is electrically coupled to the metallic plane.

19. (AMENDED) The electronic structure of claim 17, wherein the electronic structure includes at least one power plane, and wherein a thickness of the redistribution [layer] structure is large enough that a nearest distance between the solder member and any power plane of the at least one power plane is not less than a predetermined minimum distance value.

22. (AMENDED) The electronic structure of claim 21, further comprising a second metallic plane on the second surface of the substrate and a second redistribution structure having P second dielectric layers denoted as second dielectric layers 1, 2, ..., P, P second metal planes denoted as second metal planes 1, 2, ..., P, and a second microvia structure through the P second dielectric layers, wherein P is at least 1, wherein second dielectric layer 1 is on the second surface of the substrate and on the second metallic plane, wherein second metal plane J is on second dielectric layer J for J =1, 2, ..., P, wherein if I > 1 then second dielectric layer I is on second dielectric layer I-1 and on second metal [layer] plane I-1 for I = 2, ..., P, wherein the microvia structure electrically couples the second metal plane P to the second metallic plane, and wherein the second metallic plane is electrically coupled to the PTH.